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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/065,771	11/18/2002	Sreenath Mambakkam	6284.P007	2404

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EXAMINER	
FUREMAN, JARED	

ART UNIT	PAPER NUMBER
2876	

DATE MAILED: 05/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/065,771	MAMBAKKAM ET AL.	
	Examiner	Art Unit	
	Jared J. Fureman	2876	

--Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 November 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt is acknowledged of the amendment, filed on 4/29/2004, which has been entered in the file. Claims 1-21 are pending.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 10, and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Takase et al (US 6,381,513).

Re claim 1: Takase et al teaches a memory card interface apparatus comprising: a plurality of memory card interfaces (necessarily present in card machine 224), with at least a subset of the plurality of memory card interfaces configured to interface with a memory card (1) of a first type, the plurality of memory card interfaces being accessible in parallel (the plurality of memory card interfaces in card machine 224 are accessible in parallel by interface 223, so that interface 223 can read, erase, and write data to the memory cards in parallel) (see figure 16 and column 13, lines 9-18).

Re claim 10: Takase et al also teaches a system comprising: a controller circuit (228); a bus coupled to the controller circuit (for example, the bus between memory cards 1 and memory card interface 223 is coupled to the controller circuit 228 via the

memory card interface 223, see figure 16); a plurality of memory card interfaces (necessarily present in card machine 224), with at least a subset of the plurality of memory card interfaces configured to interface with a memory card (1) of a first type, the plurality of memory card interfaces being accessible in parallel (the plurality of memory card interfaces in card machine 224 are accessible in parallel by interface 223, so that interface 223 can read, erase, and write data to the memory cards in parallel) (see figure 16 and column 13, lines 9-18).

Re claim 19: Takase et al also teaches a method comprising: providing access to a plurality of memory card interfaces (necessarily present in card machine 224), with at least a subset of the plurality of memory card interfaces configured to interface with a memory card (1) of a first type; and providing parallel access to the plurality of memory card interfaces (the plurality of memory card interfaces in card machine 224 are accessible in parallel by interface 223, so that interface 223 can read, erase, and write data to the memory cards in parallel) (see figure 16 and column 13, lines 9-18).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim Rejections - 35 USC § 103

4. Claims 3, 4, 6, 7, 12, 13, 15, 16, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takase et al in view of Pua et al (US 2002/0178307 A1).

The teachings of Takase et al have been discussed above.

Takase et al fails to specifically teach wherein at least one of the memory card interfaces includes an indicator identifying a status of an operation for a respective memory reader interface; wherein the indicator includes a light indicating data is being written to a card in the respective memory card interface; wherein mechanical pins, of at least one of the plurality of memory card interfaces, are inserted directly into a backbone of the apparatus; wherein a first subset of the plurality of memory card interfaces are configured to interface with a memory card of a first type and a second subset of the plurality of memory card interfaces are configured to interface with a memory card of a second type wherein the first and second subset of memory card interfaces are accessible in parallel.

Pua et al teaches a memory card interface apparatus (adapter 10), system, and method comprising: a plurality of memory card interfaces (30), with at least a subset of the plurality of memory card interfaces configured to interface with a memory card of a first type (CompactFlash, Smart Media, SDIMMC, Memory Stick, etc.), wherein at least one of the memory card interfaces includes an indicator (35) identifying a status of an operation for a respective memory reader interface; wherein the indicator includes a light (the indicator 35 may be an LED) indicating data is being written to a card in the

respective memory card interface (the indicators 35 indicate when a card is being accessed); wherein mechanical pins, of at least one of the plurality of memory card interfaces, are inserted directly into a backbone of the apparatus (in that pins of a memory card will connect to pins of the interfaces); wherein a first subset (one of the interfaces 30, for example) of the plurality of memory card interfaces are configured to interface with a memory card of a first type and a second subset (a different one of the interfaces 30, for example) of the plurality of memory card interfaces are configured to interface with a memory card of a second type (interfaces are provided for a plurality of types of memory cards, such as CompactFlash, Smart Media, SDIMMC, Memory Stick, etc.) (see figure 1, paragraphs 22-32, and 37-39).

In view of Pua et al's teachings, it would have been obvious to one of ordinary skill in the art at the time of the invention to include, with the apparatus, system and method as taught by Takase et al, wherein at least one of the memory card interfaces includes an indicator identifying a status of an operation for a respective memory reader interface; wherein the indicator includes a light indicating data is being written to a card in the respective memory card interface; wherein mechanical pins, of at least one of the plurality of memory card interfaces, are inserted directly into a backbone of the apparatus; wherein a first subset of the plurality of memory card interfaces are configured to interface with a memory card of a first type and a second subset of the plurality of memory card interfaces are configured to interface with a memory card of a second type wherein the first and second subset of memory card interfaces are accessible in parallel, in order to provide a visual indication of the status of memory card

access and allow the use of different types of memory cards, thereby increasing the appeal of the apparatus, system and method to users who require the use of various types of memory cards.

5. Claims 5 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takase et al in view of the admitted prior art.

The teachings of Takase et al have been discussed above.

Takase et al fails to specifically teach wherein at least one of the memory card interfaces is configured to interface with a Write Once Read Many (WORM) memory card.

The admitted prior art teaches that WORM memory cards may be used to create archives of media files (see paragraph 7 of the specification).

In view of the admitted prior art, it would have been obvious to one of ordinary skill in the art at the time of the invention to include, with the apparatus, system, and method as taught by Takase et al, wherein at least one of the memory card interfaces is configured to interface with a WORM memory card, in order to allow users to create archives of media files.

6. Claims 8 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takase et al in view of Itou et al (US 6,010,066).

The teachings of Takase et al have been discussed above.

Takase et al fails to specifically teach wherein the apparatus includes a text display, wherein text on the display is manipulated using Simple Display Device commands.

Itou et al teaches a memory card interface apparatus and system (see figure 1), comprising a plurality of memory card interfaces (for cards 100, 110, and 120), a text display device (80), the text display device being a simple display device (in that the display device 80 is a small LCD for displaying text) (see figure 1 and column 4 lines 15-56).

In view of Itou et al's teachings, it would have been obvious to one of ordinary skill in the art at the time of the invention to include, with the apparatus, system, and method as taught by Takase et al, wherein the apparatus includes a text display, wherein text on the display is manipulated using Simple Display Device commands, in order to allow the user to view any text stored in a memory card, and thus, verify the contents of the memory card.

7. Claims 2, 11, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takase et al in view of Le et al (US 2003/0095386 A1).

The teachings of Takase et al have been discussed above.

Takase et al fails to specifically teach wherein at least one of the memory card interfaces is configured to read a plurality of different memory card types.

Le et al teaches a memory card interface apparatus (10), system, and method including a memory card interface (slot 13) that is configured to read a plurality of different memory card types (the slot 13 can accommodate any one of Smart Media memory card, Memory Stick flash memory, Secure Digital memory card, and MultiMedia flash memory cards) (see figures 1-5 and paragraphs 25 and 26).

In view of Le et al's teachings, it would have been obvious to one of ordinary skill in the art at the time of the invention to include, with the apparatus, system, and method as taught by Takase et al, wherein at least one of the memory card interfaces is configured to read a plurality of different memory card types, in order to eliminate restrictions as to which memory card must be placed into which interface, thus providing a more flexible system.

8. Claims 9 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takase et al as modified by Itou et al further in view of Le et al.

The teachings of Takase et al as modified by Itou et al have been discussed above.

Takase et al as modified by Itou et al fails to specifically teach wherein the text on the display is manipulated using Small Computer System Interface commands.

The teachings of Le et al have been discussed above. Le et al also teaches the use of the Small Computer Systems Interface (SCSI) (see paragraph 23).

In view of Le et al's teachings, it would have been obvious to one of ordinary skill in the art at the time of the invention to include, with the apparatus, system, and method as taught by Takase et al as modified by Itou et al, wherein the text on the display is manipulated using Small Computer System Interface commands, in order to provide compatibility with other devices using the Small Computer System Interface.

Response to Arguments

9. Applicant's arguments, see pages 7-8, of the amendment filed 4/29/2004, with respect to the rejection(s)of claim(s) 1-21 under 102(e) have been fully considered and

are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Takase et al. As discussed above, Takase et al teaches a plurality of memory card interfaces being accessible in parallel.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ono et al (US 6,722,572), Potdevin et al (US 5,679,007), Lin (US 2003/0168511), Reece (US 2003/0060085), Takase et al (US 2002/0080142), Terada et al (US 5,561,628), Tsuchide et al (JP 2000-235463 A), and Aisaka (JP 5-108905 A) all teach parallel or simultaneously accessing a plurality of memory cards.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jared J. Fureman whose telephone number is (571) 272-2391. The examiner can normally be reached on 7:00 am - 4:30 PM M-T, and every other Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael G. Lee can be reached on (571) 272-2398. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jared J. Fureman
Examiner
Art Unit 2876

May 18, 2004